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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/590,271

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Shunpei Yamazaki

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EXAMINER

JAHAN, BILKIS

ART UNIT

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PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/590,271	Applicant(s) YAMAZAKI, SHUNPEI	
	Examiner BILKIS JAHAN	Art Unit 2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 26 February 2009.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-16 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 22 August 2006 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 2/26/09 has been entered.

Initially, and with respect to claims [5], [6], [7], [13], [14], [15], note that a “Product by Process” claim is direct to the product *per se*, no matter how actually made. See *In re Thorpe et al.*, 227 USPQ 964 (CAFC, 1985) and the related case law cited therein which makes it clear that it is the final product *per se* which must be determined in a “Product by Process” claim, and do not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in “Product by Process” claims or not. As stated in Thorpe,

Even though product by process claims are limited by and defined by the process, determination of patentability is based on the product itself. *In re Brown*, 459 F.2d 1345, 1348, 162 USPQ 145, 147 (CCPA 1969); *Buono v. Yankee Maid Dress Corp.*, 77 F.2d 274, 279, 26 USPQ 57, 61 (2d. Cir. 1935).

Note that applicant has burden of proof in such cases as the above case law makes clear.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-3, 10-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jachimowicz et al (5,789,733) in view of Kimura (US 2003/0052324) A1.

Regarding claim 1, Jachimowicz et al discloses a semiconductor device (Fig. 2) comprising:

- an antenna 14 (Fig. 2, col. 3, lines 29-30), an integrated circuit 20 (Fig. 2, col. 3, lines 13-15), a light-emitting element 18 (Fig. 3, col. 3, lines 60-65), and
- wherein the antenna 14, the light-emitting element 18 and the light-receiving element 16 are electrically connected to the integrated circuit 20 on the same substrate 10 (Figures 1, 2).
- Jachimowicz et al does not explicitly disclose the light emitting element 6050 and the light receiving element each have a layer for conducting photoelectric conversion using a non-single crystal thin film; an integrated circuit comprising a thin film transistor.

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- However, Kimura discloses the light emitting element 6050 (Fig. 10B, Para. 169) and the light receiving element 6045 (Fig. 10A, Para. 167) each have a layer 5007, 5008, 5045 (Fig. 5A, Fig. 6C, Para. 125, Para. 146) for conducting photoelectric conversion using a non-single crystal thin film (Para. 125, Para. 146); an integrated circuit (Fig. 10B) comprising a thin film transistor 5026 (Fig. 6A, Para. 133). The above modification is used to control the photo electric conversion elements (Para. 4) and photo electric conversion elements can attain sufficient signal amplitude and reduce cost of the device (Para. 29). It would have been obvious to one of the ordinary skill of the art at the time of invention to add Jachimowicz's structure with Kimura's structure as suggested above to control the photo electric conversion elements (Para. 4) and photo electric conversion elements can attain sufficient signal amplitude and reduce cost of the device (Para. 29).

Regarding claim 2, Jachimowicz et al in view of Kimura discloses limitations in claim 1 above and Jachimowicz et al further discloses the integrated circuit 20, the light-emitting element 18 and the light-receiving element 16 are formed on the same substrate 10.

Regarding claim 3, Jachimowicz et al in view of Kimura discloses limitations in claim 1 above and Jachimowicz et al further discloses the antenna 14, the integrated

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circuit 20, the light-emitting element 18 and the light-receiving element 16 are formed on the same substrate 10.

Regarding claims 10, 11, Jachimowicz in view of Kimura discloses all limitations in claims 1, 2 above.

Claims 5-7, 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jachimowicz et al (5,789,733), Kimura (US 2003/0052324) and further in view of Dreifus (4,575,621).

Regarding claims 5, 6, 7, Jachimowicz et al in view of Kimura discloses limitations in claims 1, 2 above and that forming the light-emitting element and the light-receiving element over a first substrate and then separated the elements from the substrate, and attaching the elements to a second substrate, are intermediate method steps that do not affect the structure of the final device.

- Also regarding claims 5, 6, it is noted that Kimura shows all aspects of the semiconductor device according to the instant invention (see above).
- Jachimowicz et al in view of Kimura does not explicitly disclose the integrated circuit, the light emitting element and the light receiving element are formed on the second substrate.
- However, Dreifus discloses the integrated circuit 6 (Fig. 3, col. 8, line 21), the light emitting element 8 (Fig. 3, col. 8, line 40) and the light receiving

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element 10 (Fig. 3, col. 7, lines 42-45) are formed on the second substrate (Figures 3, 4). Dreifus teaches the above modification is used to transmit and receive information to and from each other (col. 3, lines 12-14). It would have been obvious to one of the ordinary skill of the art at the time of invention to replace Jachimowicz in view of Kimura's structure with Dreifus's structure as suggested above to transmit and receive information to and from each other (col. 3, lines 12-14).

Regarding claims 13-15, Jachimowicz in view of Kimura and Dreifus discloses all limitations above in claims 1, 2, 5 and that forming the integrated circuit, the light-emitting element and the light-receiving element over a first substrate and then separated the first substrate and attaching a second substrate, are intermediate method steps that do not affect the structure of the final device.

- Also regarding claims 13-15, it is noted that Kimura shows all aspects of the IC card according to the instant invention (see above).

Claims 4, 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jachimowicz et al (5,789,733), Kimura (US 2003/0052324) A1 in view of Nishi et al (US 6,590,633 B1).

Regarding claims 4, 12, Jachimowicz modified by Kimura discloses some limitations in claims 1, 2 above and Jachimowicz modified by Kimura further discloses

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the integrated circuit comprising a connection terminal and, a rectification circuit (Kimura, Fig. 14B, element “AMPLIFICATION ELEMENT”) that generates power supply voltage from an alternating current signal that is input to the connection terminal by an antenna 2708 (Fig. 13G, Para. 190). However, Kimura does not disclose a demodulation circuit and a logic circuit.

- ❖ However, Nishi et al disclose a demodulation circuit (col. 12, line 27) and a logic circuit (col. 12, line 20). Nishi teaches a demodulation circuit and logic circuit are used to management and control of the charging state and the management and control of the communication port (col. 12, lines 22-24). It would have been obvious to one of the ordinary skill of the art at the time of invention to add Kimura’s structure with Nishi’s structure including demodulation circuit and logic circuit to manage and control charging state and the communication port (col. 12, lines 22-24).

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jachimowicz et al (5,789,733), Kimura (US 2003/0052324) and further in view of Nishi et al (US 6,590,633 B1) and Dreifus (4,575,621).

Regarding claim 8, Jachimowicz modified by Kimura and Dreifus discloses some structural limitations above in claims 4, 5 and Dreifus further discloses the integrated circuit 6 (Dreifus, Fig. 3, col. 8, line 21), the light emitting element 8 (Dreifus, Fig. 3, col.

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8, line 40) and the light receiving element 10 (Dreifus, Fig. 3) formed integrally (Dreifus, Figures 3, 4).

Claims 9, 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jachimowicz et al (5,789,733), Kimura (US 2003/0052324) Dreifus (4,575,621) and further in view of Nakamura (US 2004/0152392 A1).

Regarding claims 9, 16, Jachimowicz in view of Kimura and Dreifus discloses limitations above and Kimura further discloses the first substrate is a glass substrate 5001 (Fig. 5A, Para. 118) but does not disclose the second substrate is a plastic substrate.

- However, Nakamura discloses the second substrate is a plastic substrate 315 (Fig. 3A, Para. 127). Nakamura teaches plastic substrate is used to emit light from the light emitting elements (Para. 28, lines 1-2). It would have been obvious to one of the ordinary skill of the art at the time of invention to add Jachimowicz in view of Kimura's structure with Nakamura's structure including plastic substrate to emit light from the light emitting elements (Para. 28, lines 1-2).

Response to Arguments

Applicant's arguments with respect to claim 1-16 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to BILKIS JAHAN whose telephone number is (571)270-5022. The examiner can normally be reached on M-F, 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571)-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Wai-Sing Louie/
Primary Examiner, Art Unit 2814

BJ